Resistive SiC-MESFET Mixer

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***Abstract*—A single-ended silicon carbide resistive MESFET mixer was designed and characterized. The mixer has a minimum conversion loss of 10.2 dB and an input third order intercept point of 35.7 dBm at 3.3 GHz.**

***Index Terms*—High-level mixer, intermodulation distortion, intermodulation intercept point, resistive mixer, S-band, silicon carbide, wide bandgap semiconductors.**

I. Introduction

THE major motivation for using microwave transistors processed on wide bandgap materials, such as silicon carbide (SiC) and gallium nitride, has traditionally been their capability to handle high power densities. This has been demonstrated in high-power amplifiers operating in the L-, S-, and X-bands using SiC MESFETs [1]. Of great importance in radar and communications systems is also the dynamic range; this is especially true in wideband systems. Wide bandgap materials offers both good power performance and dynamic range. Earlier work has been done on silicon carbide Schottky diode high-level mixers [2], [3], but none has been reported on FET devices.

II. SiC MESFETs

The transistors were processed in-house. The MESFET epistructure was grown on a semi-insulating 4H-SiC substrate by Cree, Inc. The MESFET structure consists of a 0.35 μm p-buffer with $N_A = 5 \cdot 10^{15}$ cm^{-3}, a 0.4 μm channel with $N_D = 2 \cdot 10^{17}$ cm^{-3}, and a 0.15 μm cap-layer with $N_D = 1.1 \cdot 10^{19}$ cm^{-3}. The process steps are: mesa and recess etching, ohmic contact formation, oxidation, sputtering of dielectrics, definition of gates with EBL, pad formation, passivation, air-bridge formation, and dicing. The mesa and recess were defined by dry etching using a CF_4/O_2 plasma. Ohmic contacts were formed by annealing nickel at 1000 °C. The gate length is 0.5 μm and the gate metallization is Au/Pt/Ti. The devices are passivated with Si_3N_4.

The saturated drain current, I_{dss}, is 160 mA/mm and the dc-transconductance, g_m, is 24 mS/mm. The on-resistance, r_{ch}, is 23 $\Omega \cdot$ mm. From S-parameter measurements on a 200 μm MESFET, an extrinsic transit frequency, $f_{T,ext}$, of 6.3 GHz and a maximum frequency of oscillation, $f_{\max}$, of 37 GHz at a V_{ds} of 40 V were calculated. The Class A output power were measured with load-pull at 3 GHz and $V_{ds} = 80$ V. The power density is 1.6 W/mm (measured for a gate width of 0.4 mm). The device used in this experiment has 16 gate fingers 200 of μm each, thus having a total gate width of 3.2 mm.

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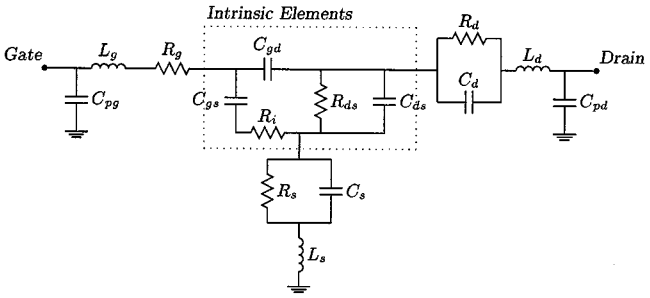

Fig. 1. Small-signal equivalent circuit.

TABLE I
EXTRACTED MODEL PARAMETERS

C_{pg} [fF]	47	L_g [pH]	0
C_{pd} [fF]	47	L_d [pH]	17
C_{ds} [fF]	240	$R_{ds,min}$ [Ω]	0.1
C_{gd} [fF]	248	$R_{ds,max}$ [Ω]	$2.18 \cdot 10^5$
C_{gs} [fF]	239	V_{pk} [V]	-0.29855
C_s [fF]	890	p_1	1.6079
C_d [fF]	410	p_2	1.0772
R_s [Ω]	2.5	p_3	0.38216
R_d [Ω]	3.1	p_4	0.061671
R_i [Ω]	0.001	p_5	0.003727
R_g [Ω]	1	η [Ω]	1

III. Device Modeling

The device is modeled using a lumped-element, large-signal model. The model is valid for the non saturated region and accounts for the channel conductance as a function of applied gate voltage, which should be sufficient for a resistive mixer operating at low frequency (S-band).

The equivalent small-signal circuit is shown in Fig. 1. The small-signal model used in this work differs from standard models; the drain and source resistances are replaced by a resistance in parallell with a capacitance. This empirical model accounts for the observed frequency dependence in the source and drain resistances. The main purpose of this model is to describe the S-parameters as a function of applied gate-voltage rather than have a strong connection to device physics.

The parasitic pad capacitances are extracted using a standard procedure [4]. The remaining parasitic elements are extracted using an optimization procedure.

The channel conductance as a function of gate voltage is described by the following model

$$R_{ds} = R_{ds,\min} + \frac{R_{ds,\max}}{1 + \eta^{-1} R_{ds,\max}(1 + \tanh\psi)} \quad (1)$$

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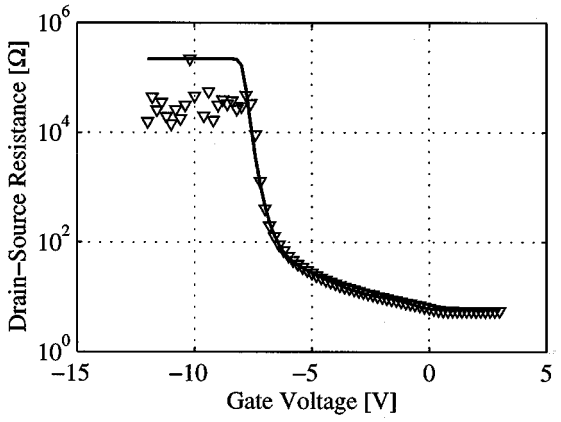

Fig. 2. Drain-source resistance versus gate voltage; solid (model) and markers (measurements).

where

$$\psi = p_1 (V_{gs} - V_{pk}) + p_2 (V_{gs} - V_{pk})^2 + p_3 (V_{gs} - V_{pk})^3 + \cdots \quad (2)$$

η is an arbitrary constant, added for consistency and is set to 1 Ω. $R_{ds,\min}$ and $R_{ds,\max}$ are the minimum and maximum measured drain-source resistances (after subtracting the parasitic resistances R_s and R_d); the remaining parameters are extracted using an optimization procedure. The extracted value of R_i is so small that its effect is negligeble and thus the equivalent circuit could be simplified. Extracted model parameters are shown in Table I. In Fig. 2, modeled and measured drain-source resistance is plotted versus gate bias. Drain-source resistance is measured by taking the real part of the output port impedence i.e., S_{22} converted to Z-domain.

IV. Design

The mixer is designed to work as a downconverter within the S-band, with an LO frequency of 3.0 GHz and an input RF frequency of 3.3 GHz. The mixer topology is identical to that first proposed by Maas [5]. The LO is applied to the gate; two open stubs acts as impedence matching and also short circuits the RF signal. The RF is applied to the drain through a two section coupled Chebysheff bandpass filter; an open stub is used as impedence matching and for shortcircuiting the LO signal. The IF signal is extracted at the drain through high impedence line and a low-pass filter. Radial stubs are used at the gate-bias and IF ports as bandstop filters for the LO and RF signals, respectively.

The circuit is fabricated on a soft substrate (IsoClad, $\epsilon_r = 2.33$), the circuit is gold-plated and soldered to a copper plate. The SiC-MESFET is glued to a patch (grounded to the backside by vias) and wire bonded into the circuit. A drawback with this simple type of mounting is that the bond wires tend to be long, almost 1.5 mm and that the thermal management is poor. A photograph of the fabricated mixer is shown in Fig. 3.

V. Measurements

The conversion loss (CL) versus gate bias was measured for an LO of 3.0 GHz and an RF of 3.3 GHz (Fig. 4). Optimum gate bias for minimum CL was found to be −6.7 V. The CL was then

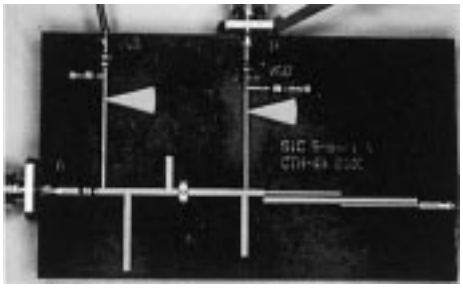

Fig. 3. Photograph of the fabricated mixer. The LO and RF ports are to the left and right, respectively; the IF port is at the top.

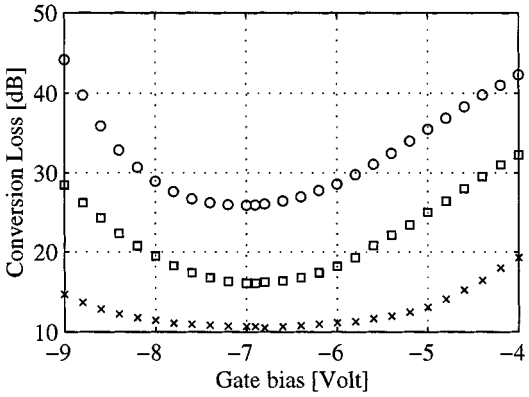

Fig. 4. Conversion loss versus gate bias for different LO powers: 5.4 dBm (circles), 15.3 dBm (squares), and 25.2 dBm (crosses). Input RF power was 0 dBm.

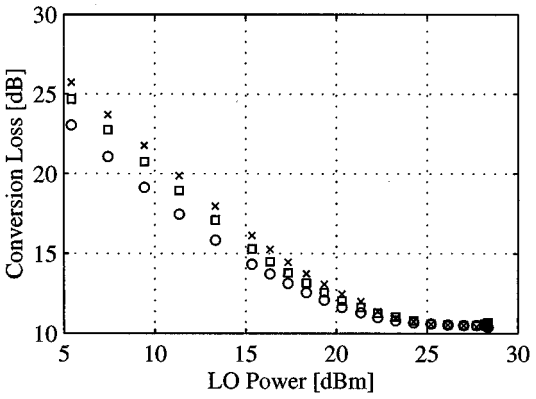

Fig. 5. Conversion loss versus LO power for different RF powers: 10 dBm (circles), 15 dBm (squares), and 18 dBm (crossses).

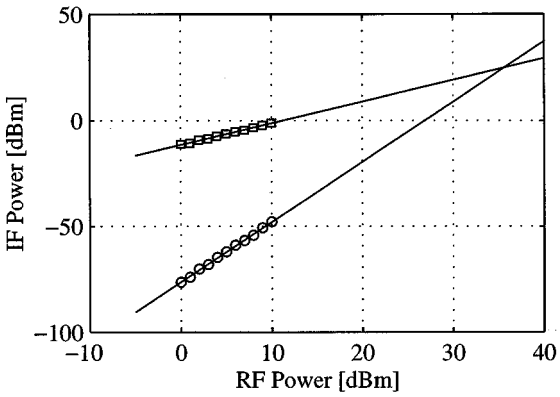

Fig. 6. Third-order intermodulation products. Input LO power was 27 dBm.

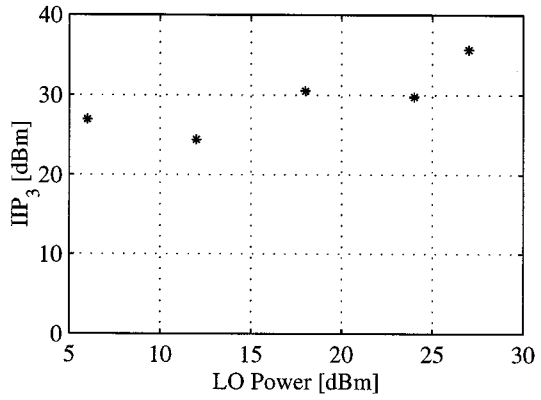

Fig. 7. Measured IIP_3 versus LO power.

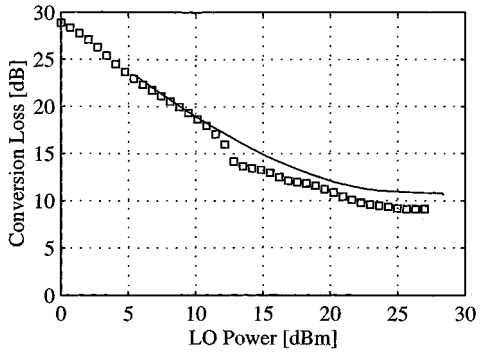

Fig. 8. Simulated CL versus LO power; squares (simulations), solid (measurements).

measured versus LO power (Fig. 5), with the gate bias kept at the optimum value of -6.7 V.

The third order intermodulation intercept point (IIP_3) was measured using a two-tone measurement. The two, equal-power, RF input signals are separated by 10 MHz ($f_{RF1} = 3290$ Mhz, $f_{RF2} = 3300$ Mhz). The RF power was limited to 11 dBm; thus, the 1 dB compression point could not be reached. Maximum IIP_3 measured was 35.7 dBm at an LO power of 27 dBm (Fig. 6). The IIP_3 are measured for different LO power (Fig. 7). The figure shows that the mixer has not reached saturation, this indicates that more available LO power could give even higher IIP_3.

The measurements are compared to harmonic balance simulations performed in the software ADS from Agilent (Fig. 8).

VI. Conclusion

A single-ended resistive SiC-MESFET mixer was designed and characterized. A conversion loss of 10.2 dB and an IIP_3 of 35.7 dBm were measured at 3 GHz. This is, to our knowledge, the best result reported for any resistive FET/HEMT mixer. It is our belief that conversion loss can, by more careful mixer design, be reduced to at least 6 dB. The mixer was not optimized for low intermodulation, thus making further improvements possible.

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